Improved Quality-Factor of 0.18-μm CMOS Active Inductor by a Feedback Resistance Design

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***Abstract*—A novel CMOS active inductor approach, which can improve the quality-factor, was presented in this report. A cascode-grounded active inductor circuit topology with a feedback resistance was proposed, which can substantially improve its equivalent inductance and quality-factor. This feedback resistance active inductor was implemented by using a 0.18-μm 1P6M CMOS technology, which demonstrates a maximum quality-factor of 70 with a 5.7-nH inductance at 1.55 GHz, where the self-resonate frequency is 2.5 GHz. The dc power consumption of this active inductor is less than 8 mW.**

***Index Terms*—Active inductor, CMOS, quality-factor.**

I. Introduction

In THE near decade, for the increasing demands of wireless personal communication system, low cost and high integration process technologies are required to reduce the production cost and the system dimension. According to these requirements, CMOS technologies has become the best choice for wireless communication systems operating below 5 GHz. However, an important issue using standard CMOS technologies in MMIC designs is the microwave signal loss from their low-resistivity silicon substrates. With this lossy silicon substrate, the spiral inductors cannot easily achieve good performances by CMOS technologies. In the recent years, several research groups have demonstrated the integration of spiral inductors on silicon substrates with quality-factors in the range of 3$\sim$10 using multi-level spirals [1] or high-resistivity substrates [2], [3]. Another solution is using bonding wires to replace the spiral inductor, but this approach is limited to a few circuit topologies with barely any process control. An alternative method, which hasn't been studied intensively, is to implement an inductor by CMOS MMIC active devices, where the equivalent inductive impedance can be generated. The main advantages of this active inductor include the higher quality-factor, reducing chip area and potentially tunable characteristics, which can be applied on the on-chip filters, matching networks, and LC tank circuits. However, the limited operation frequency range, higher noise figure, and dc power consumption are there major drawbacks. Reports which have been attempted on this subject mainly addressed GaAs-based technologies [4] [5] in the past. A few works have carried out active inductors by CMOS technologies [6]–[9], but very few papers demonstrated the measured results. In this report, a new CMOS high quality-factor active inductor architecture is proposed and characterized.

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II. Active Inductor Design

The most common active inductor topology is the grounded active inductor. This circuit topology is based on the gyrator theory, containing only two transistors, which generate an inductive impedance. This architecture of active inductors is possible to obtain several nH of inductance operating at a few GHz region. For achieving a higher inductance and a higher quality-factor, a cascode circuit topology has been proposed to reduce the output conductance (g_{ds}) [7] by CMOS technologies. In the schematics shown in Fig. 1(a), without the resistance R_f, is the so-called cascode-grounded active inductor, by adding a transistor M_2 stacks on top of the M_3 to reduce the equivalent conductance. By reducing the g_{ds} in transistor M_3, the equivalent resistance decreased, and the equivalent inductance increased, as described in [7]. In order to further enhance the inductance and quality-factor of this active inductor, a feedback resistance R_f has been added between M_1 and M_2 in this report, as shown in Fig. 1(a). The feedback resistance R_f forms an additional inductive reactance of the impedance looking into the source terminal of M_1 [10], which can significantly increase the inductance of cascode-grounded active inductor. Furthermore, the increased inductance also results in an increased quality-factor. The equivalent circuit model of the added R_f active inductor is shown in Fig. 1(b), including three parameters, C_{gs}, g_{ds}, and g_m, to analyze this circuit, and the values of each component are expressed below.

$$C_{eq} = C_{gs3} \tag{1}$$

$$G_{eq} = \frac{2g_{ds2} + R_f g_{ds2}^2}{R_f g_{ds2} + 1} \tag{2}$$

$$R_{eq} = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2[g_{m2}C_{gs1}^2 - g_{m1}C_{gs1}C_{gs2}(R_f g_{ds2} + 1)]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{3}$$

$$L_{eq} = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2}\,(R_f g_{ds2} + 1)}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2}. \tag{4}$$

In (3) and (4), the effect of feedback resistance is $(R_f g_{ds2} + 1)$, which is designed to be a value larger than unity. By decreasing the equivalent resistance R_{eq}, with the help from the R_f, also results in an increase of the equivalent inductance L_{eq}. Therefore, the inductance and quality-factor can be improved in consequence. Based on these equations, the simulated one-port S-parameters are shown in Fig. 2, which illustrates that by introducing this feedback resistance in the CMOS active inductor

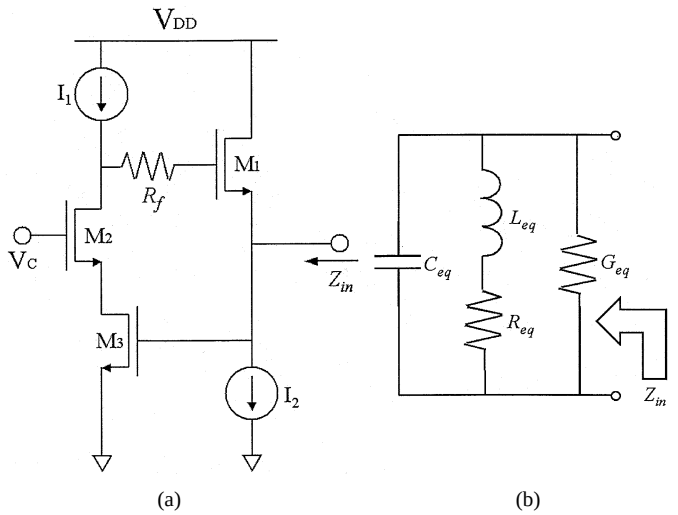


Fig. 1. (a) Schematics of cascode-grounded active inductor with a feedback resistance; (b) equivalent circuit model of this active inductor.

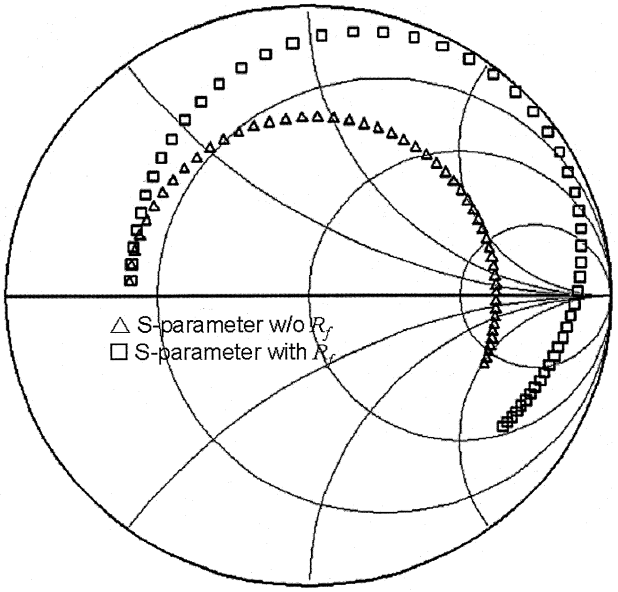


Fig. 2. Simulated S-parameters of a feedback resistance active inductor (with R_f) and a cascode-grounded active inductor (without R_f); the frequency region is from 100 MHz to 3.1 GHz.

design, the characteristics can be enhanced as compared with the original cascode-grounded active inductor approach, where the feedback resistance is not involved.

III. Characteristics of Feedback Resistance Active Inductor

This active inductor was fabricated by a 0.18-μm 1P6M standard CMOS process, where all transistors, M_1, M_2, and M_3, were 50-μm channel wide n-MOSFETs to provide sufficient g_m, C_{gs}, and g_{ds}. The performance of both the feedback resistance and cascode-grounded (without feedback resistance, R_f) active inductors were first simulated by our homemade 0.18-μm scalable CMOS RF large-signal model, where the additional substrate parasitics are included in this model. The simulated quality-factors and inductances are shown in Fig. 3. Max-

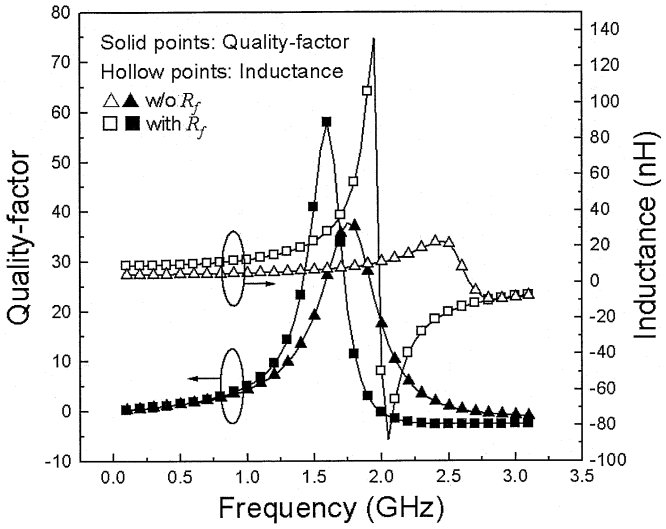
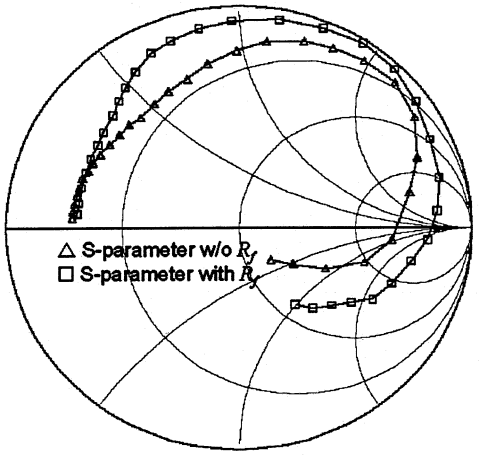
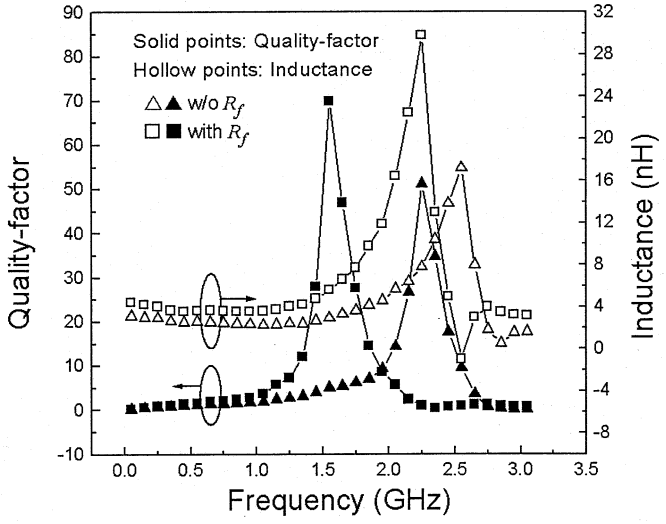


Fig. 3. Simulated quality-factor and inductance of a feedback resistance active inductor (with R_f) and a cascode-grounded active inductor (without R_f).



(a)



(b)

Fig. 4. (a) Measured S-parameters of a feedback resistance active inductor (with R_f) and a cascode-grounded active inductor (without R_f). (b) The measured quality-factor and inductance of feedback resistance active inductor and cascode-grounded active inductor.

imum simulated quality-factors of feedback resistance and cascode-grounded (without R_f) active inductors are 60 and 36, corresponding to an inductance of 10 nH and 5 nH, respectively. Because of the increased inductance, the self-resonate frequency of feedback resistance active inductor becomes lower, i.e., 2.0 GHz versus 2.7 GHz.

The measured S-parameters, which demonstrate the same trend as the simulated results, were carried out by a network analyzer. According to the measured results, the equivalent inductance and quality-factor can be easily obtained from the one port S-parameters. Fig. 4(a) shows the one-port S-parameters of both with and without feedback resistance active inductors, and these measured characteristics are similar to the predictions of derivated equations, shown in Fig. 2, where the improved performance can be obtained by adding the feedback resistance. Fig. 4(b) illustrates the measured quality-factor and inductance of feedback resistance and cascode-grounded (without R_f) active inductors. The supplied voltage V_{DD} of this active inductor is 2 V with a 4-mA dc current, and the total power consumption is 8 mW. The maximum quality-factor of feedback resistance active inductor is 70 at 1.55 GHz with a 5.7-nH inductance and the self-resonate frequency is 2.5 GHz. As for the CMOS active inductor, without the feedback resistance, these values are 51 at 2.2 GHz and the self-resonate frequency is 2.8 GHz. Due to the additional parasitic effects, the measured inductances are smaller than simulation ones. To compare with spiral inductors from the same standard CMOS process, spiral inductors with multilayer interconnects were also fabricated. Spiral inductors demonstrate the same inductance between 5 and 7 nH, where the quality-factor is between 6 and 7.5. The active inductor achieves much higher quality-factor but a lower self-resonate frequency. In the meantime, this active inductor requires only 88×90 μm^2 chip area, which is much smaller than the on-chip spiral inductors.

IV. Conclusions

This report demonstrates a high quality-factor CMOS active inductor with a novel configuration by a 0.18-μm CMOS technology. By introducing a feedback resistor R_f to a cascode-grounded active inductor, the inductance and quality-factor can be enhanced by this approach. The maximum quality-factor is 70 corresponding to an inductance of 5.7 nH, where this active inductor also consumes 8-mW dc power.

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